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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,371	02/26/2004	YI-JEN CHAN	11955-US-PA	2370
31561	7590	10/12/2006	EXAMINER	
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE			NGUYEN, LINH V	
7 FLOOR-1, NO. 100			ART UNIT	
ROOSEVELT ROAD, SECTION 2			PAPER NUMBER	
TAIPEI, 100			2819	
TAIWAN			DATE MAILED: 10/12/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/708,371	<b>Applicant(s)</b> CHAN ET AL.	
	<b>Examiner</b> Linh V. Nguyen	<b>Art Unit</b> 2819	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 August 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 February 2004 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. This office action is in response to communication filed on 8/9/06. Claims 1 – 15 are pending on this office action.

#### ***Specification***

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

#### ***Response to Arguments***

3. Applicant's arguments filed 8/9/06 have been fully considered but they are not persuasive.

With respect to claim 1, under remarks applicant argued, "the present invention discloses that the input power terminal and the output terminal are different terminals. Thus there exists a distinction between Ishikawa's feedback manner and applicant's teaching, ". Examiner respectfully disagrees because Fig. 5 of Ishikawa from prior office action clearly teaches the input power terminal (A) and the output terminal (RF out) of the power amplifier transistor (Tr2) are different terminals and does not disclosed any feedback manner.

With respect to claim 7, applicant used the same reasons stated above, to argued Ishikawa reference does not discloses "an active bias circuit connected to the power output device and the gate of the power amplifier transistor for receiving an input

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power from the output power device and providing a gate bias voltage to the gate”.

Examiner respectfully disagrees from the following:

From previous office action, Fig. 1 of Ishikawa et al discloses an integrated circuit for a power amplifier (Tr2) with an active bias circuit (4), comprising: a power output device (output terminal of 3); a power amplifier transistor (Tr2) with a gate (Gate of Tr2) connected to a gate bias voltage (voltage bias B of 4); an active bias circuit (4) connected to the power output device (output terminal 3) and the gate of the power amplifier transistor (gate of Tr2) for receiving an input power (A) from the power output device (output terminal of 3) and providing a gate bias voltage (B) to the gate (gate of Tr2), wherein the gate bias voltage (4) is increased corresponding to an increase of the input power (Col. 12 lines 22 – 28); and a power input device (input terminal of 3) connected to an output terminal (output terminal of Tr2) of the power amplifier transistor (Tr2) for receiving an amplified output power (amplified output power of Tr2) from the power amplifier transistor (Tr2).

From Fig. 5 above, Ishikawa et al. clearly teaches an active bias circuit (4) connected to the power output device (3) and the gate of the power amplifier transistor (Tr2) for receiving an input power (3) from the output power device (3) and providing a gate bias voltage (B) to the gate (gate of Tr2).

With respect to claim 13, applicant argued “Ishikawa reference does not discloses” a method for generating a gate bias voltage of a power transistor corresponding to an input power, ... outputting a gate bias voltage corresponding to the

input power, wherein the gate bias voltage is increased corresponding to an increased of the input power". Examiner respectfully disagrees from the following:

Fig. 1 and fig. 5 of Ishikawa et al. clearly teaches method for generating a gate bias voltage (B) of a power amplifier transistor (Tr2) corresponding to an input power (A), comprising: providing an input power (A); and outputting a gate bias voltage (B) corresponding to the input power (A), wherein the gate bias voltage is increased corresponding to an increase of the input power (Col. 12 lines 22 – 28).

Ishikawa per discussed above, disclosed every aspect of applicant's claimed invention. Therefore, the same rejection from previous office action is applying to this office action.

#### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1- 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishikawa et al. U.S. patent No. 5,982,236.

Regarding claim 1, Fig. 5 of Ishikawa et al. discloses a power amplifier (Tr2) with an active bias circuit (4), comprising: a power amplifier transistor (Tr2)) with a gate (gate of Tr2) connected to a gate bias voltage (B); and an active bias circuit (4) connected to an input power terminal (A) and the gate of the power amplifier transistor

(Gate of Tr2 ) for receiving an input power (output of 3) from the input power terminal (A) and outputting the gate bias voltage (B), to the gate wherein the gate bias voltage (gate of Tr2) is increased corresponding to an increase of the input power (Col. 12 lines 25 – 30) .

Regarding claim 4, wherein the power amplifier transistor (Tr2) and the active bias circuit (4) is manufactured by a system on chip process (Fig. 1).

Regarding claim 5, wherein the active bias circuit (4) comprises a diode (D11) and a resistor (R11, R12).

Regarding claim 6, wherein an equivalent resistance of the diode in the active bias circuit varies in correspondence with the input power (this is an inherent characteristic of diode transistor D11, because the output of D11 varies according to RF input power (A) therefore the equivalent resistance of D11 must be varies according to power input A).

Regarding claim 7, Fig. 1 of Ishikawa et al Fig. 1 of Ishikawa et al discloses an integrated circuit for a power amplifier (Tr2) with an active bias circuit (4), comprising: a power output device (output terminal of 3); a power amplifier transistor (Tr2) with a gate (Gate of Tr2) connected to a gate bias voltage (voltage bias B of 4); an active bias circuit (4) connected to the power output device (output terminal 3) and the gate of the power amplifier transistor (gate of Tr2) for receiving an input power (A) from the power output device (output terminal of 3) and providing a gate bias voltage (B) to the gate (gate of Tr2), wherein the gate bias voltage (4) is increased corresponding to an increase of the input power (Col. 12 lines 22 – 28); and a power input device (input



terminal of 3) connected to an output terminal (output terminal of Tr2) of the power amplifier transistor (Tr2) for receiving an amplified output power (amplified output power of Tr2) from the power amplifier transistor (Tr2).

Regarding claim 10, wherein the power amplifier transistor and the active bias circuit is manufactured by a system on chip process (Fig. 1).

Regarding claim 11, wherein the active bias circuit (4), comprises a diode (D11) and a resistor (R11, R12).

Regarding claim 12, wherein the equivalent resistance of the diode in the active bias circuit varies in correspondence with the input power (this is an inherent characteristic of diode transistor D11, because the output of D11 varies according to RF input power (A) therefore the equivalent resistance of D11 must be varies according to power input A).

Regarding claim 13, Fig. 1 Ishikawa et al. discloses method for generating a gate bias voltage (B) of a power amplifier transistor (Tr2) corresponding to an input power (A), comprising: providing an input power (A); and outputting a gate bias voltage (B) corresponding to the input power (A), wherein the gate bias voltage is increased corresponding to an increase of the input power (Col. 12 lines 22 – 28).

Regarding claims 2-3, 8-9 and 14 – 15, wherein a curve of an increase of the gate bias voltage versus the input power is a linear or non-linear curve. However Ishikawa et al. as applied to claims 1, 7 and 13 above disclosed the voltage bias for power amplifier transistor Tr2 is increase or decreasing according to increase or decrease of the Power input terminal A; therefore the curve of increase of the gate bias

voltage of Ishikawa et al. must be either in the form of linear or non-linear curve. Furthermore Fig. 13(b) discloses a linear and non-linear curve of Pout at the power input terminal A; hence, voltage bias increase or decrease according to increase or decrease of linear or non-linear of Pout; thereby, voltage bias (B) of power amplifier Tr2 must be increase or decrease linear or non-linear accordingly to increase or decrease of linear or non-linear of Pout at input power terminal A.

### ***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

### ***Contact Information***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571)



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272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Rexford Barnie can be reached at (571) 272-7492. The fax phone numbers for the organization where this application or proceeding is assigned are (571-273-8300) for regular communications and (571-273-8300) for After Final communications.

LINH NGUYEN  
PRIMARY EXAMINER

10/4/06

Linh Van Nguyen

A handwritten signature in black ink, appearing to read 'Linh Van Nguyen', with a long horizontal flourish extending to the right.

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